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**Lab 2 Report – Combinational Network Design**

**July 5, 2015**

**Objective**

The purpose of this lab was to learn how to design a combinational logic network using Quartus II. The design is first made as a truth table in the prelab and the two logic design networks are entered into the software. The design is then simulated through ModelSim-Altera to interpret and analyze the input and output waveforms and verified on the DE2 board. For the second part, the design is simulated using a counter clocked at 27 MHz and again verified on the DE2 board.

**Design and Test Procedure**

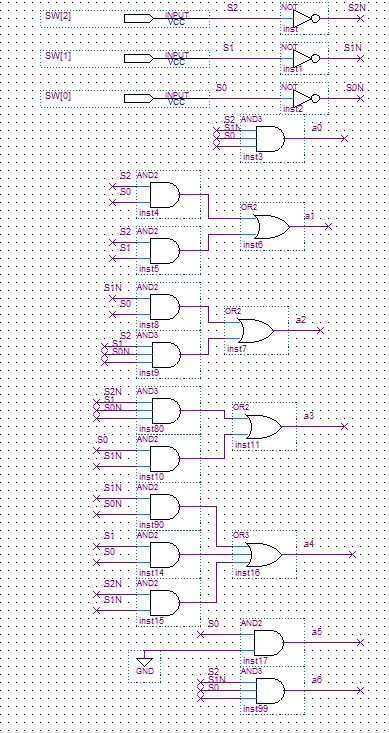
The problem for this lab instructed us to come up with equations to light up and darken the specified segments of the seven segment display. For this there are two equations and we can use either. The equations were found in the prelab of this lab (Prelab attached at the back). The equations which are equal are the sum of products (SOP) and products of sum (POS).

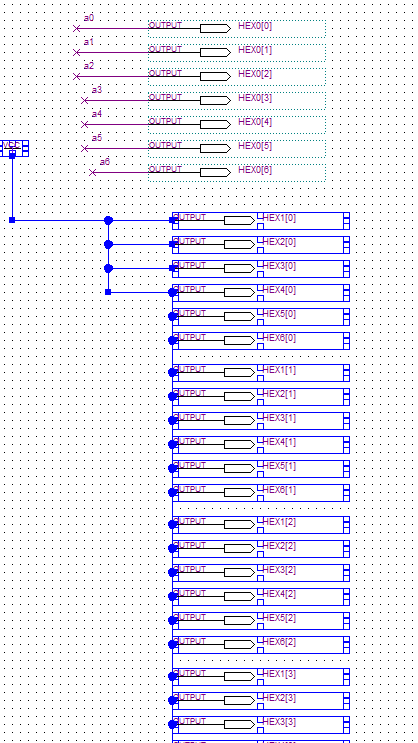
Part 1: For this part of the lab, we took the equations of SOP and POS and used the Quartus II software to implement it using various combinations of gates (AND, OR), inputs and outputs.

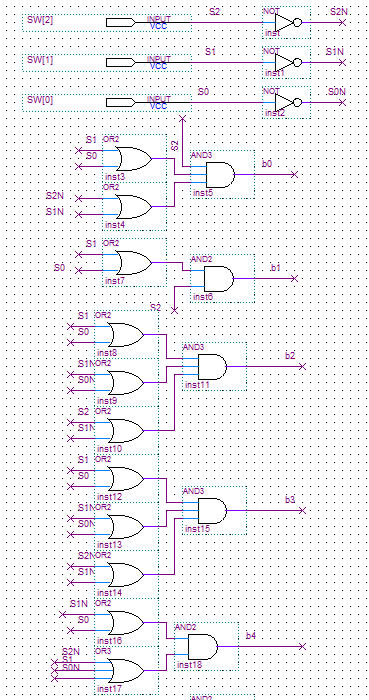
(The screenshots of the design are given over the next two pages. The first two are collectively the SOP and the next two are the POS design.)

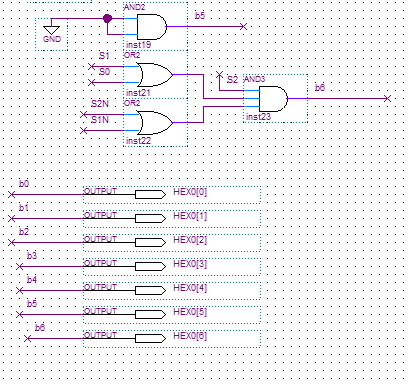
The procedure consisted of using the gates and implementing the equations found in the prelab. Once the design was implemented, it was required to see the input and output waveforms in ModeSim-Altera. For this the designs were exported to the software and run and the desired waveforms were verified.

Part 2: For part two only the input to the design changed, using a counter to generate the input signals for S2, S1 and S0 from 0 to 7 in binary, so we see each output by 1 increment on the DE2 board.

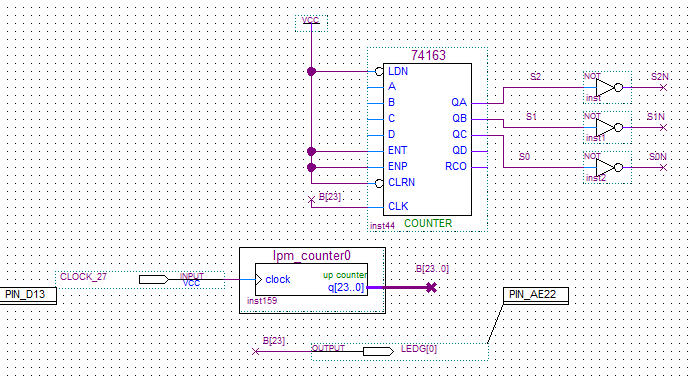


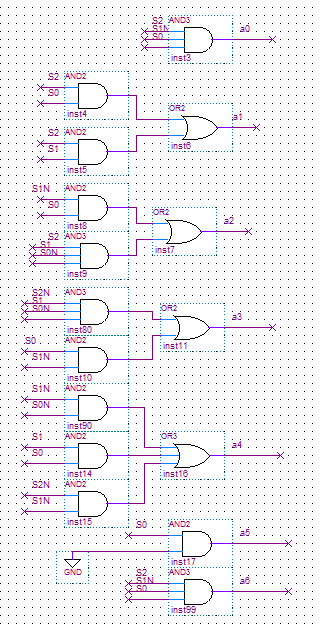


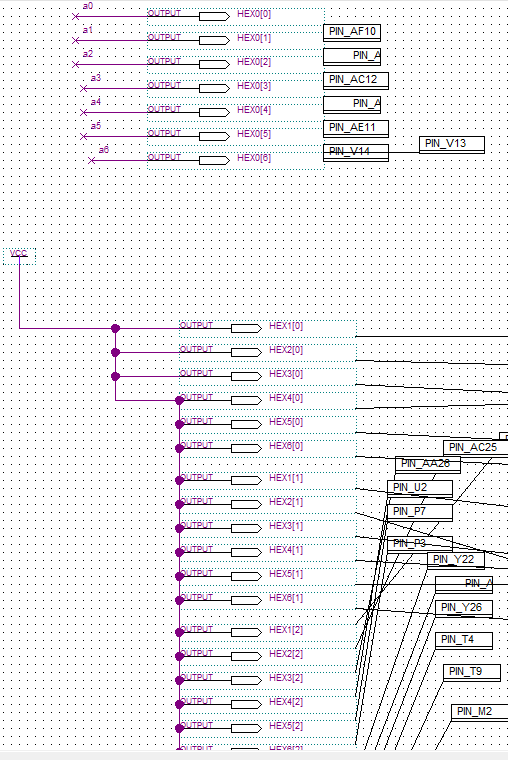


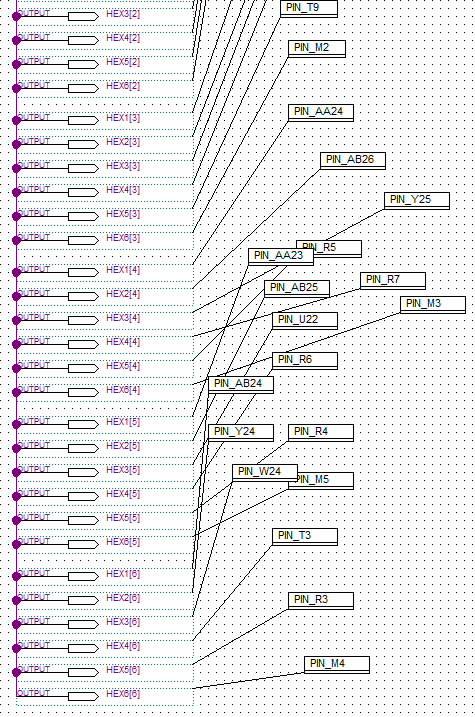


Part 2 screenshots are as follows:





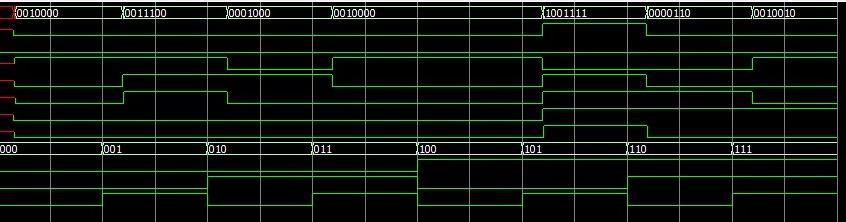




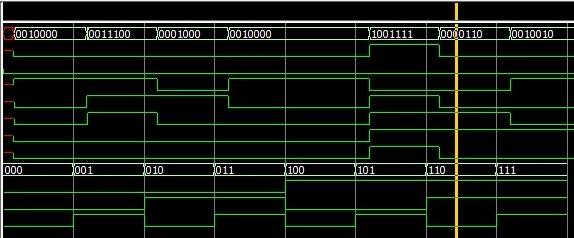
**Results:**

The waveforms of the two designs are given below:

The waveform of SOP is as follows:



The waveform of POS is as follows:



The results are as expected. Each segment of the display lit up when required hence, this showed that the equations and designs required no debugging. The concept of gate delay was also demonstrated as seen in the graphs, as each time an input value changed, there was a delay in the change of the output. However, the delay was not noticed visually.

**Conclusions:**

This lab shows the implementation of a gate design also shows that the POS and SOP designs, both have the same output. Also the concept of gate delay was proved practically through the waves as seen in the simulation with ModelSim-Altera.